

POWER CHIP SCALE PACKAGE

ABSTRACT OF THE DISCLOSURE

A packaging arrangement for a semiconductor device including a leadframe and a die coupled thereto. The die is coupled to the leadframe such that its back surface
5 (drain area) is coplanar with source leads and a gate lead extending from the leadframe. A
stiffener is coupled to the leadframe and electrically isolated therefrom in order to help
maintain the position of the source and gate pads of the leadframe. When the semiconductor
device is coupled to a printed circuit board (PCB), the exposed surface of the die serves as the
direct drain connections while the source leads and gate leads serve as the connections for the
10 source and gate regions of the die.

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